16V/20W High-Integration, High-Efficiency Power Solution for Wireless Power Transmitter

FEATURES

- Input Voltage Range: 4V-16V
- Up to 20W Power Transfer
- Integrated High Efficiency Full-Bridge Power Stage
- Integrated High Efficiency 5V-1ABuck Convertor
- Optimized for EMI
- Build in 3.3V-200mA LDO
- Provide 2.5V Voltage Reference
- Integrated Input Current sense with ±2% accuracy for FOD and modulation
- 3.3V and 5V PWM Signal compatible
- Input Under-Voltage Lockout
- Over current protection
- Thermal shutdown
- 3mm*4mm QFN-19L Package
- Friendly for PCB layout

APPLICATIONS

- WPC Compliant Wireless Chargers of 7.5W to 15W Systems for Mobiles, Tablets and Wearable devices
- General Wireless Power Transmitters for Consumer, Industrial and Medical Equipment
- Proprietary Wireless Chargers and Transmitters

DESCRIPTION

The SCT63240 is a highly integrated power solution optimized for wireless power transmitter applications. This product can be combined with a specialized controller or general MCU based transmitter controller to achieve high performance, high efficient and cost effective wireless power transmitter system which compliant with WPC specification.

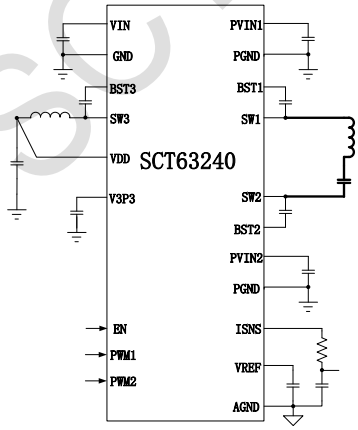
This device integrates all the power functions in a wireless power transmitter including Full bridge power stage，5V Buck converter, 3.3V LDO and input current sensing to simplify system design and minimize external components thus improve system efficiency.

The integrated Full bridge supports up to 20W power transfer and ensures efficient switching with EMI emission. The build in 5V buck convertor and 3.3V LDO provide power rails to transmitter controller and external equipment and also the power stage driver inside. The build in current detection circuits provides input current information with ±2% accuracy to support FOD(Foreign Object Detection) and current modulation.

The SCT63240 has built-in protection features including input under-voltage lockout, power stage over current protection and short-circuit protection, and thermal shutdown protection.

The SCT63240 is available in an 19-pin flip chip QFN 3mm*4mm package.

TYPICAL APPLICATION



DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT63240FIAR	63240	QFN-19L

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	24	V
PVIN1, PVIN2	-0.3	19	V
SW1,SW2	-1	19	V
SW3	-1	24	V
BST1,BST2	-0.3	25	V
BST3	-0.3	30	V
BST1-SW1,BST2-SW2,BST3-SW3	-0.3	6	V
VDD, V3P3, VREF, ISNS, EN, PWM1, PWM2	-0.3	6	V
Operating junction temperature TJ(2)	-40	125	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

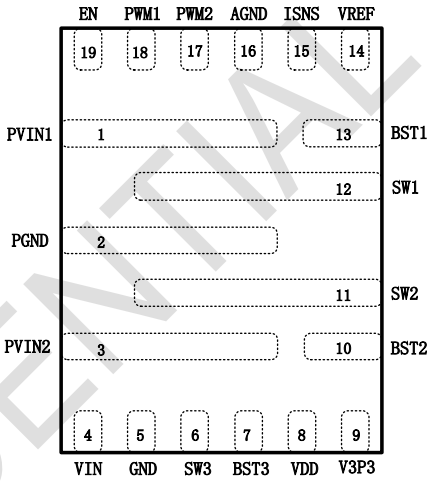


Figure 1. Top view 19-Lead QFN 3mm*4mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
PVIN1	1	Input supply voltage of half-bridge FETs Q1 and Q2. Connected to the drain of high side FET Q1. a local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
PGND	2	PGND is the common power ground of full bridge, connected to the source terminal of low side FETs Q2 and Q4 internally.
PVIN2	3	Input supply voltage of half-bridge FETs Q3 and Q4. Connected to the drain of high side FET Q1. Local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
VIN	4	Input supply voltage of buck convertor. A local bypass capacitor from VIN pin to GND pin should be added. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
GND	5	Power ground of buck convertor.
SW3	6	Regulator switching output. Connect SW3 to an external power inductor.
BST3	7	Power supply bias for the high-side power MOSFET gate driver of buck convertor. Connect a 0.1uF capacitor from BST3 pin to SW3 pin.

VDD	8	Buck convertor 5V output voltage, connect 22uF capacitor from this pin to GND. VDD is also the power supply for gate driver of power stage and as the input power for 3.3V LDO.
V3P3	9	3.3V LDO output. Connect 1uF capacitor to ground.
BST2	10	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
SW2	11	Switching node of the half-bridge FETs Q3 and Q4, as shown in the block diagram.
SW1	12	Switching node of the half-bridge FETs Q1 and Q2, as shown in the block diagram.
BST1	13	Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin.
VREF	14	Output of the 2.5V LDO. connect 1uF capacitor to ground.
ISNS	15	Current detection output. The voltage of the pin is proportional to the input current.
AGND	16	Analog ground of the IC
PWM2	17	PWM logic input to the FET Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q4, and turns on the high-side FET Q3. Logic LOW turns off the high-side FET Q3 and turns on the low-side FET Q4. When PWM input is in the tri-state mode, both Q3 and Q4 are turned off.
PWM1	18	PWM logic input to the FET Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q2, and turns on the high-side FET Q1. Logic LOW turns off the high-side FET Q1 and turns on the low-side FET Q2. When PWM input is in the tri-state mode, both Q1 and Q2 are turned off.
EN	19	Chip enable pin. Pull the pin high or keep it floating to enable the IC. When chip enable, Buck convertor will start to work if VIN higher than UVLO threshold. After VDD is established, power stage can respond to PWM input logic then.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4	20	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-19L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	42	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	45	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63240 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink

that is soldered to the leads of the SCT63240. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=V_{PVIN1}=V_{PIN2}=12V, VDD=5V, T_J=-40°C~85°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
V_{IN}	Operating input voltage		4		16	V
V_{IN_UVLO}	Input UVLO Threshold Hysteresis	V_{IN} rising		3.6 400		V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0V, VIN=12V		1	2	μA
I_{SHDN_PVIN}	Shutdown current from PVIN1,PVIN2	EN=0V, PVIN=12V		1	2	uA
I_{SHDN_VDD}	Shutdown current from VDD	EN=0V, VDD=5V		1	2	uA
I_{VINQ}	Quiescent current from VIN pin	EN floating, VDD=5.5V, no switching, no loading on Buck and LDO		120		uA
I_{PVINQ}	Quiescent current from PVIN1, PVIN2	EN floating, VDD=5.5V, no switching, no loading on Buck and LDO		50		uA
I_Q	Quiescent current from VDD pin	EN floating, VDD=5.5V, no switching, no loading on Buck and LDO		200		uA
ENABLE INPUTS and PWM logic						
V_{EN_H}	Enable high threshold			1.18		V
V_{EN_L}	Enable low threshold			1.1		V
V_{IH}	PWM1, PWM2 Logic level high	V3P3=3.3V, VDD=5V	2.65			V
V_{IL}	PWM1, PWM2 Logic level low	V3P3=3.3V, VDD=5V			0.55	V
V_{TS}	PWM1, PWM2 Tri-state voltage		1.2		2	V
T_{THOLD}	Tri-state activation time			60		ns
Buck convertor						
F_{SW}	Switching frequency			600		KHz
V_{DD}	Output voltage		4.95	5	5.05	V
I_{LIM_HS}	High-side power MOSFET peak current limit threshold			1.5		A
t_{SS}	Internal soft-start time			1		ms
3.3V LDO						
V_{3P3}	Output voltage	Cout=1uF, VDD=5V, T_A=25℃	3.2	3.3	3.4	V
I_{3P3}	Output current Capability		200			mA
I_{SC}	Short current			50		mA
2.5V REFFERENCE OUTPUT						
V_{2P5}	Output voltage reference		2.45	2.5	2.55	V
I_{3P3}	Output current Capability		100			mA
I_{SC}	Short current			50		mA
Current Sense						
V_{ISNS0}	Voltage with no input current	I_{PVIN}=0A ,Tj=25℃		0.6		V
V_{ISNS1}	Voltage with 1A input current	I_{PVIN}=1A, Tj=25℃		1.2		V

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{ISNS2}	Voltage with 1.6A input current	I_{PVIN}=1.6A, Tj=25℃		2.2		V
R_{ISNS}	Input current to output voltage gain	$V_{ISNS}=V_{ISNS0}+I_{PVIN}*R_{ISNS}$		1		V/A
Protection						
T_{SD}	Thermal shutdown threshold Hysteresis	T_J rising		155 35		°C °C

TYPICAL TEST RESULTS

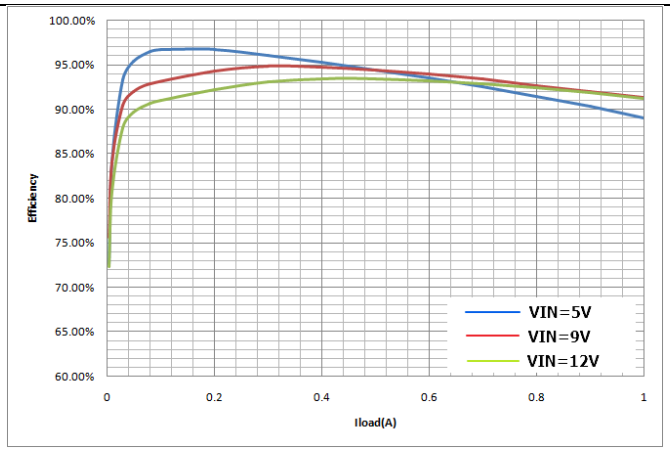


Figure 2. 5V-buck Efficiency vs Iload

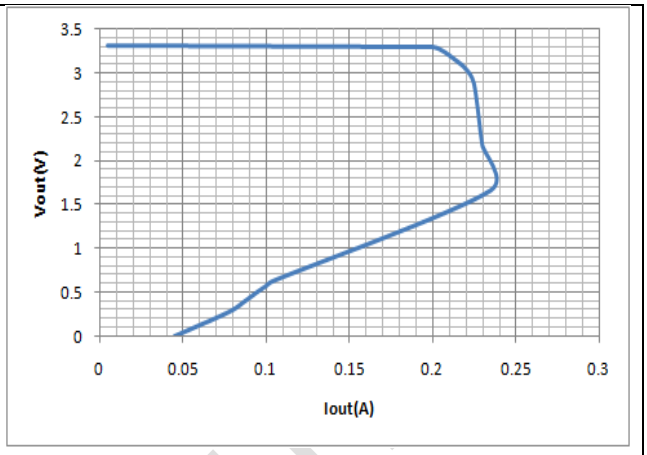


Figure 3. 3.3V LDO Iout vs Vout

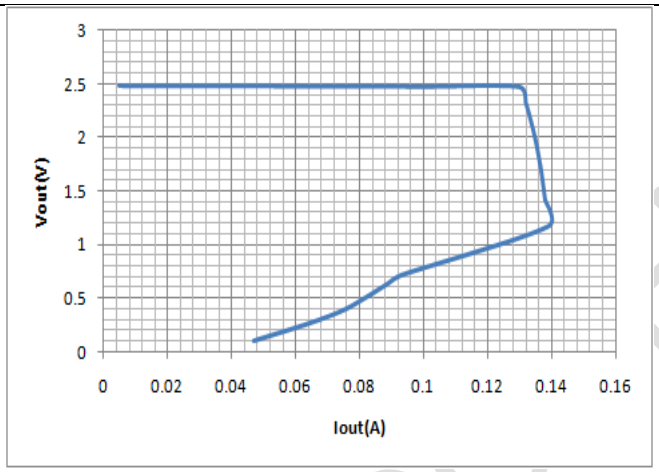


Figure 4. 2.5V LDO Iout vs Vout

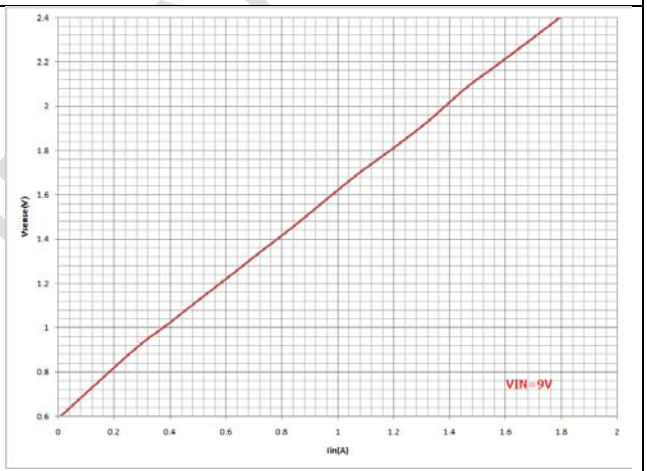


Figure 5. Current sense output voltage vs Iin

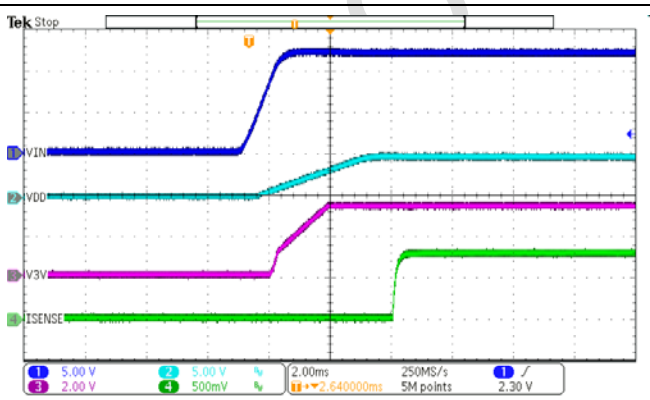


Figure 6. VIN=12V Power Up

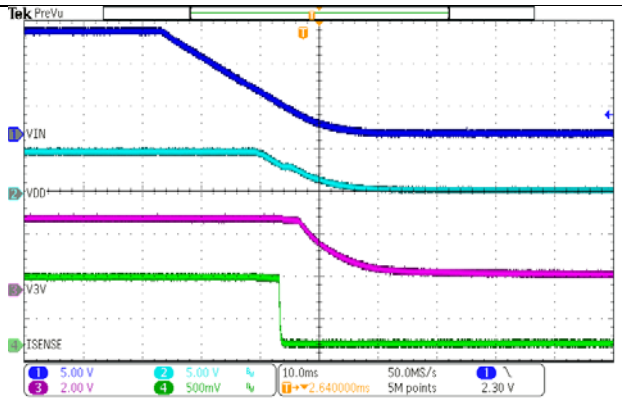


Figure 7. VIN=12V Power Down

TYPICAL TEST RESULTS

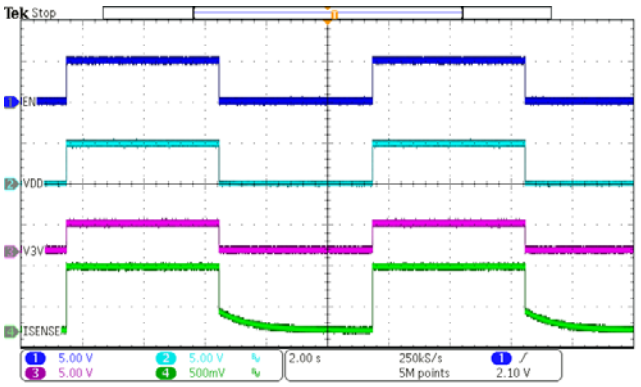


Figure 8. Enable and Disable

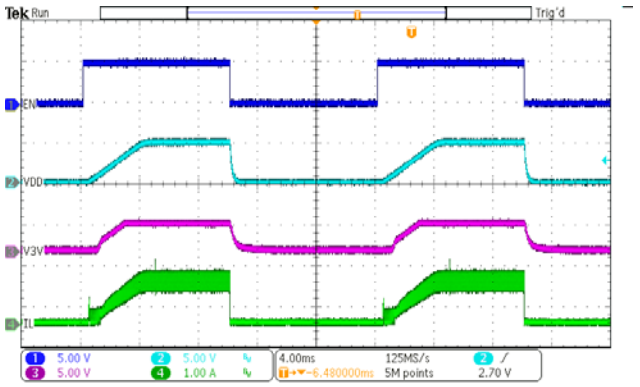


Figure 9. Enable and Disable

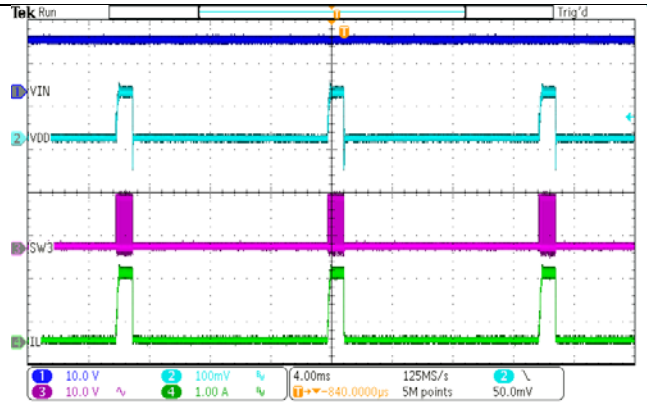


Figure 10. 5V-BUCK hard short test

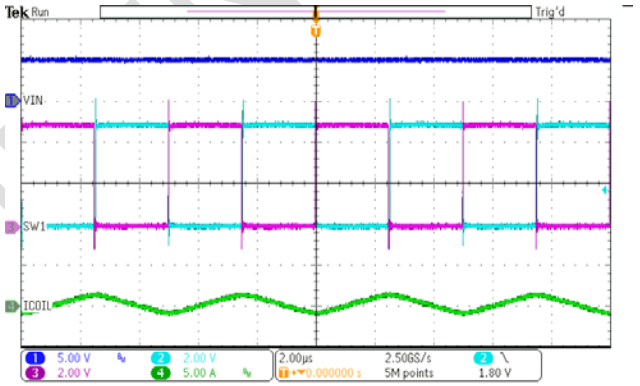


Figure 11. Full bridge Vin=5V

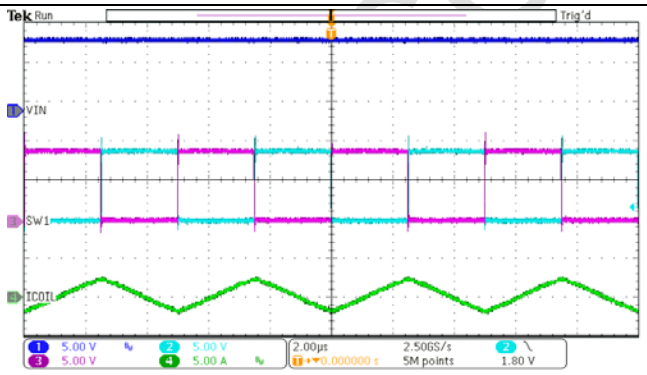


Figure 12. Full bridge Vin=9V

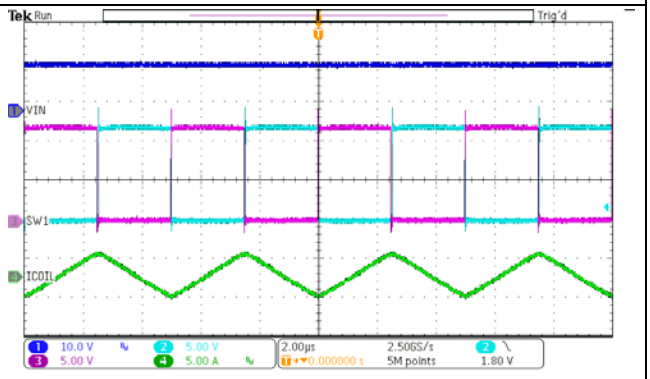


Figure 13. Full bridge Vin=12V

FUNCTIONAL BLOCK DIAGRAM

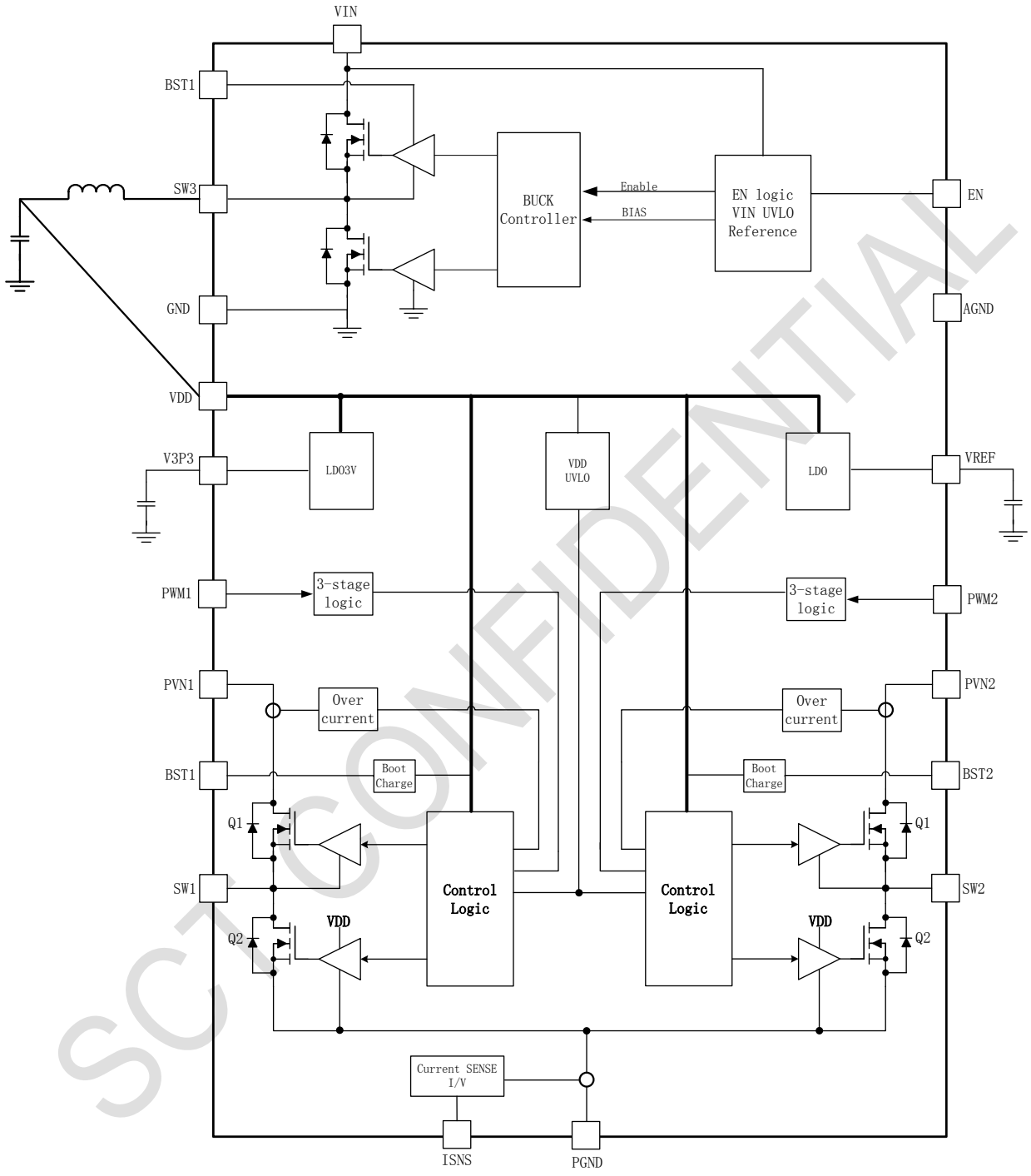
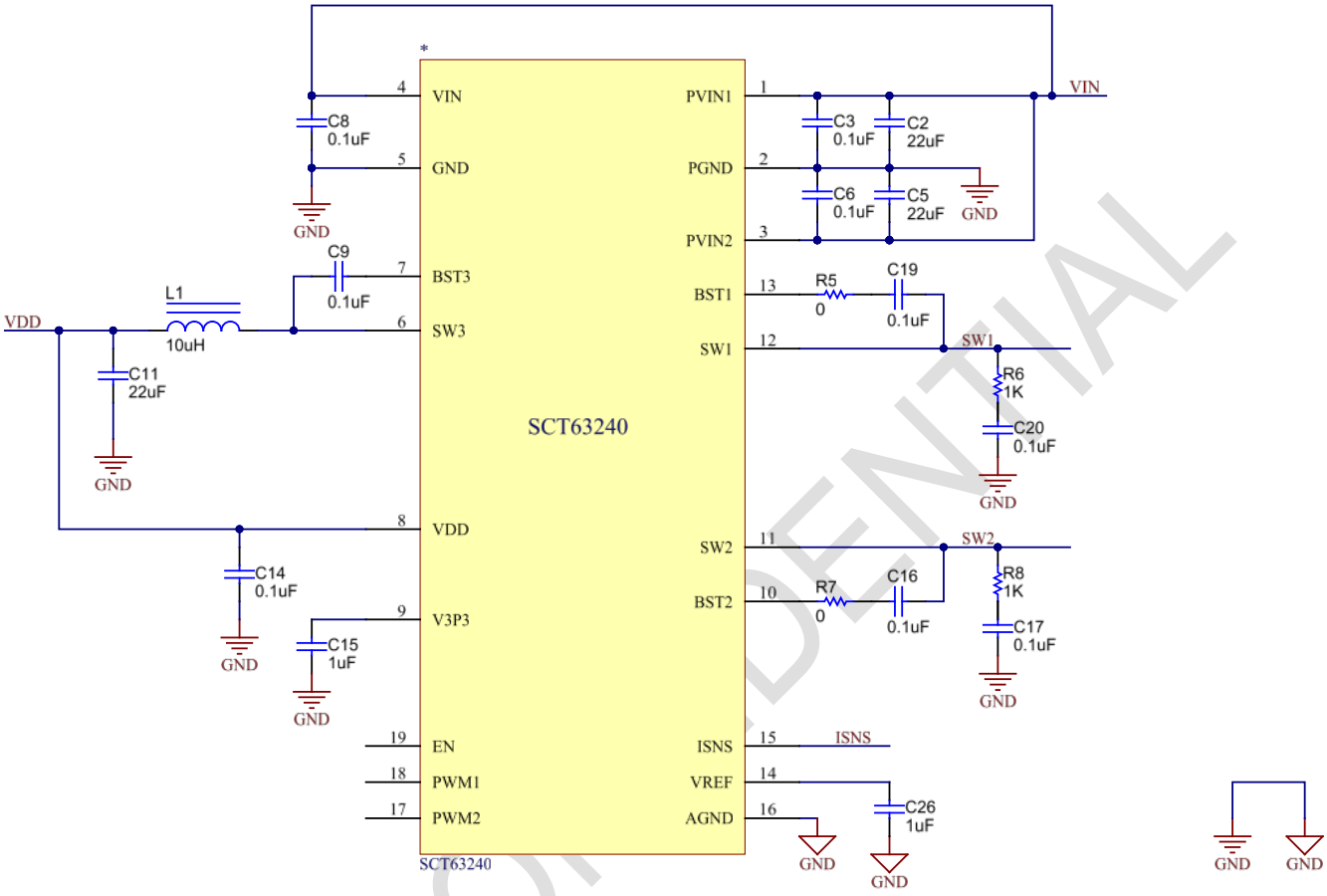


Figure 14. Functional Block Diagram

APPLICATION INFORMATION

Typical Application



Layout Guideline

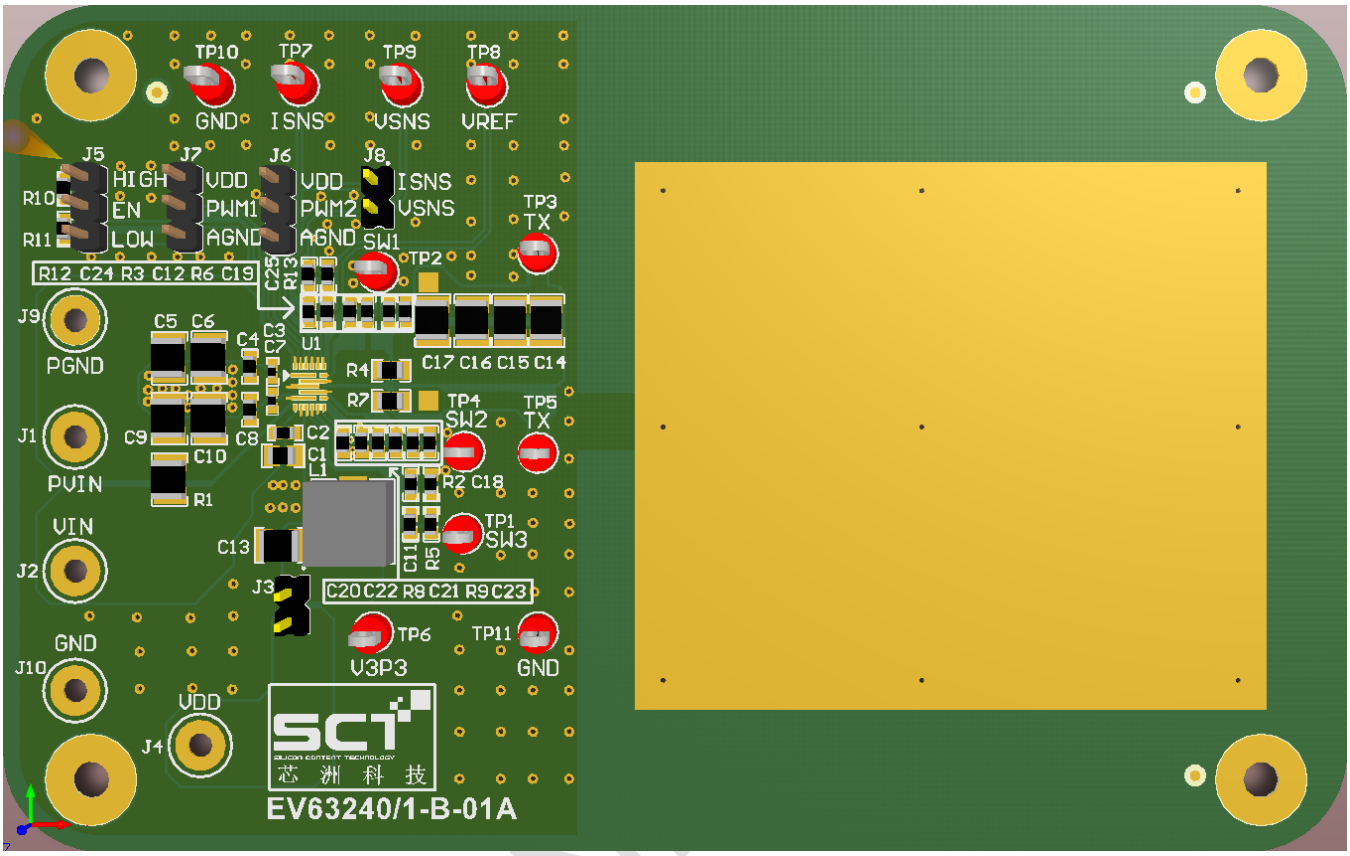
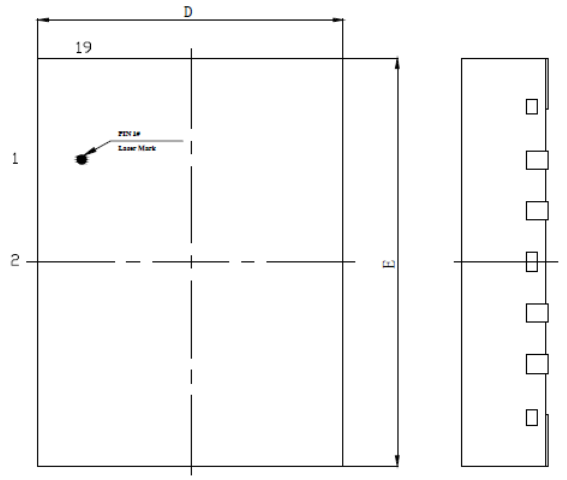
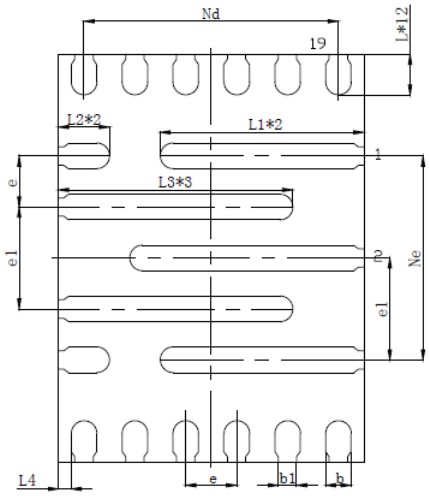


Figure 15. PCB Layout Example

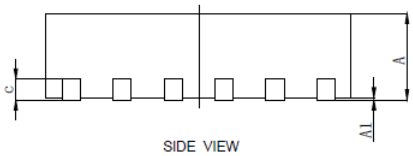
PACKAGE INFORMATION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	2.90	3.00	3.10
Nd		2.50BSC	
Ne		2.00BSC	
e		0.50BSC	
e1		1.00BSC	
E	3.90	4.00	4.10
L	0.35	0.40	0.45
L1	1.95	2.00	2.05
L2	0.45	0.50	0.55
L3	2.25	2.30	2.35
L4	0.075	0.125	0.175